Data Sheet No. PD60259

IRS2453D(S)PbF

SELF-OSCILLATING FULL-BRIDGE DRIVER IC

Features

- Integrated 600 V full-bridge gate driver
- CT, RT programmable oscillator
- 15.6V Zener clamp on V_{CC}
- Micropower startup
- Logic level latched shutdown pin
- Non-latched shutdown on CT pin (1/6th V_{CC})
- Internal bootstrap FETs
- Excellent latch immunity on all inputs & outputs
- ESD protection on all pins
- 14-lead SOIC or PDIP package
- 1.0 µs (typ.) internal deadtime

Description

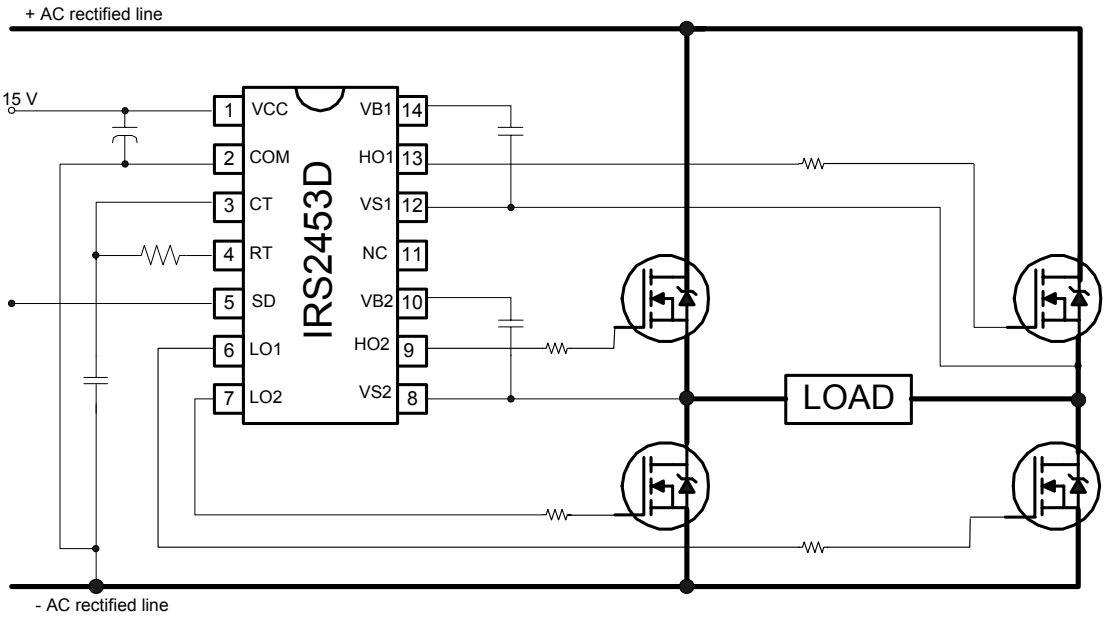
The IRS2453D is based on the popular IR2153 self-oscillating half-bridge gate driver IC, and incorporates a high voltage full-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Noise immunity is achieved with low di/dt peak of the gate drivers, and with a undervoltage lockout hysteresis greater than 1.5 V. The IRS2453D also includes latched and non-latched shutdown pins.

Packages

14 Lead PDIP
IRS2453DPbF

14 Lead SOIC (Narrow Body)
IRS2453DSPbF

Typical Connection Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Parameter				
Symbol	**Definition**	**Min.**	**Max.**	**Units**
V_{B1}, V_{B2}	High side floating supply voltage	-0.3	625	V
V_{S1}, V_{S2}	High side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO1}, V_{HO2}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{LO1}, V_{LO2}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{RT}	R_T pin voltage	-0.3	V_{CC} + 0.3	
V_{CT}	C_T pin voltage	-0.3	V_{CC} + 0.3	
V_{SD}	SD pin voltage	-0.3	V_{CC} + 0.3	
I_{RT}	R_T pin current	-5	5	mA
I_{CC}	Supply current (Note 1)	---	25	
dV_S/dt	Allowable offset voltage slew rate	-50	50	V/ns
P_D	Maximum power dissipation @ $T_A \leq +25$ ºC, 8-Pin DIP	---	1.0	W
P_D	Maximum power dissipation @ $T_A \leq +25$ ºC, 8-Pin SOIC	---	0.625	
$R_{\theta JA}$	Thermal resistance, junction to ambient, 8-Pin DIP	---	125	ºC/W
$R_{\theta JA}$	Thermal resistance, junction to ambient, 8-Pin SOIC	---	200	
T_J	Junction temperature	-55	150	ºC
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6 V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Parameter		Min.	Max.	Units
Symbol	Definition			
V_{BS1}, V_{BS2}	High side floating supply voltage	V_{CC} - 0.7	V_{CLAMP}	V
V_{S1}, V_{S2}	Steady state high side floating supply offset voltage	-3.0 (Note 2)	600	
V_{CC}	Supply voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	Supply current	(Note 3)	5	mA
T_J	Junction temperature	-25	125	ºC

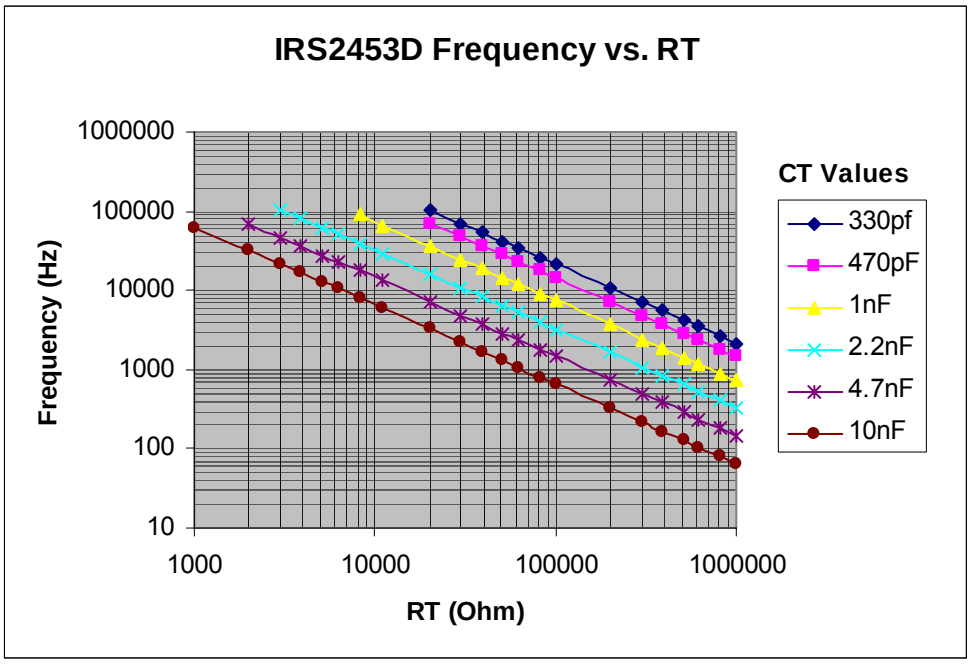
Note 2: Care should be taken to avoid output switching conditions where the V_S node flies inductively below ground by more than 5 V.

Note 3: Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6 V zener diode clamping the voltage at this pin.

Recommended Component Values

Parameter		Min.	Max.	Units
Symbol	Component			
R_T	Timing resistor value	1	---	kΩ
C_T	C_T pin capacitor value	330	---	pF

VBIAS (VCC, VBS) = 14 V, VS=0 V and TA = 25 °C, CLO1=CLO2 = CHO1=CHO2 = 1 nF.



Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 14 V, C_T = 1 nF and T_A = 25 °C unless otherwise specified. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO. CLO1=CLO2=CHO1=CHO2=1 nF.

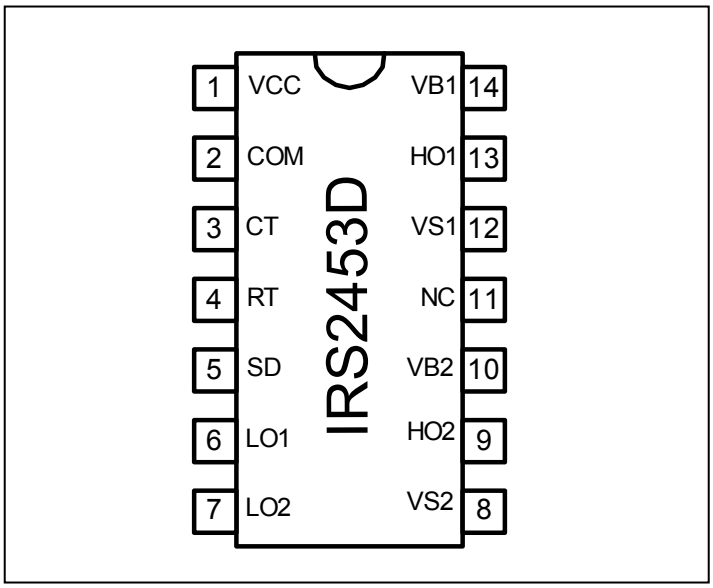
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Voltage Supply Characteristics						
V_{CCUV+}	Rising V_{CC} undervoltage lockout threshold	10.0	11.0	12.0	V	
V_{CCUV-}	Falling V_{CC} undervoltage lockout threshold	8.0	9.0	10.0		
$V_{CCUVHYS}$	V_{CC} undervoltage lockout hysteresis	1.5	2.0	2.4		
I_{QCCUV}	Micropower startup V_{CC} supply current	---	140	200	µA	$V_{CC} \le V_{CCUV-}$
I_{QCC}	Quiescent V_{CC} supply current	---	1.3	2.0	mA	
I_{CC_20K}	V_{CC} supply current at f_{osc} (R_T = 36.5 kΩ)	---	3.0	3.5		
I_{CCFLT}	V_{CC} supply current when SD > V_{SD}	---	360	500	µA	
V_{CLAMP}	V_{CC} Zener clamp voltage	14.6	15.6	16.6	V	I_{CC} = 5 mA
Floating Supply Characteristics						
I_{QBS1UV}, I_{QBS2UV}	Micropower startup V_{BS} supply current	---	3	10	µA	$V_{CC} \le V_{CCUV-}$, $V_{CC} = V_{BS}$
I_{QBS1}, I_{QBS2}	Quiescent V_{BS} supply current	---	30	100		
V_{BS1UV+}, V_{BS2UV+}	V_{BS} supply undervoltage positive going threshold	8.0	9.0	10.0	V	
V_{BS1UV-}, V_{BS2UV-},	V_{BS} supply undervoltage negative going threshold	7.0	8.0	9.0		
$I_{LK1, ILK2}$	Offset supply leakage current	---	---	50	µA	V_B = V_S = 600 V
Oscillator I/O Characteristics						
f_{OSC}	Oscillator frequency	19.6	20.2	20.8	kHz	R_T = 36.5 kΩ
		88	94	100		R_T = 7.15 kΩ
d	R_T pin duty cycle	48	50	52	%	f_o < 100 kHz
I_{CT}	C_T pin current	---	0.05	1.0	µA	
I_{CTUV}	UV-mode C_T pin pulldown current	1	5	---	mA	V_{CC} = 7 V
V_{CT+}	Upper C_T ramp voltage threshold	---	9.3	---	V	
V_{CT-}	Lower C_T ramp voltage threshold	---	4.7	---		
V_{RT+}	High level R_T output voltage, V_{CC} - V_{RT}	---	10	50	mV	I_{RT} = 100 µA
		---	100	300		I_{RT} = 1 mA
V_{RT-}	Low level R_T output voltage	---	10	50		I_{RT} = 100 µA
		---	100	300		I_{RT} = 1 mA
V_{RTUV}	UV-mode R_T output voltage	---	0	100		$V_{CC} \le V_{CCUV-}$

Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 14 V, C_T = 1 nF and T_A = 25 °C unless otherwise specified. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO. CLO1=CLO2=CHO1=CHO2=1 nF.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver Output Characteristics						
V_{OH}	High level output voltage, V_{BIAS} - V_O	---	V_{CC}	---	V	I_O = 0 A
V_{OL}	Low level output voltage, V_O	---	COM	---		
V_{OL_UV}	UV-mode output voltage, V_O	---	COM	---		I_O = 0 A, $V_{CC} \leq V_{CCUV-}$
t_r	Output rise time	---	120	200	ns	
t_f	Output fall time	---	50	100		
t_{sd}	Shutdown propagation delay	---	250	---		
t_d	Output deadtime (HO or LO)	0.8	1.0	1.40	μs	
I_{O+}	Output source current	---	180	---	mA	
I_{O-}	Output sink current	---	260	---		
Shutdown						
V_{SD}	Shutdown threshold at SD pin (latched)	1.8	2.0	2.3	V	
V_{CTSD}	C_T voltage shutdown threshold (non latched)	2.2	2.3	2.5		
V_{RTSD}	SD mode R_T output voltage, V_{CC} - V_{RT}	---	10	50	mV	I_{RT} = 100 μA, V_{CT} = 0 V
		---	100	300		I_{RT} = 1 mA, V_{CT} = 0 V
Bootstrap FET Characteristics						
V_{B1_ON} V_{B2_ON}	V_B when the bootstrap FET is on	13.7	14.0	---	V	
I_{B1_CAP} I_{B2_CAP}	V_B source current when FET is on	40	55	---	mA	C_{BS}=0.1 μF
$I_{B1\_10\ V}$ $I_{B2\_10\ V}$	V_B source current when FET is on	10	12	---		V_B=10 V

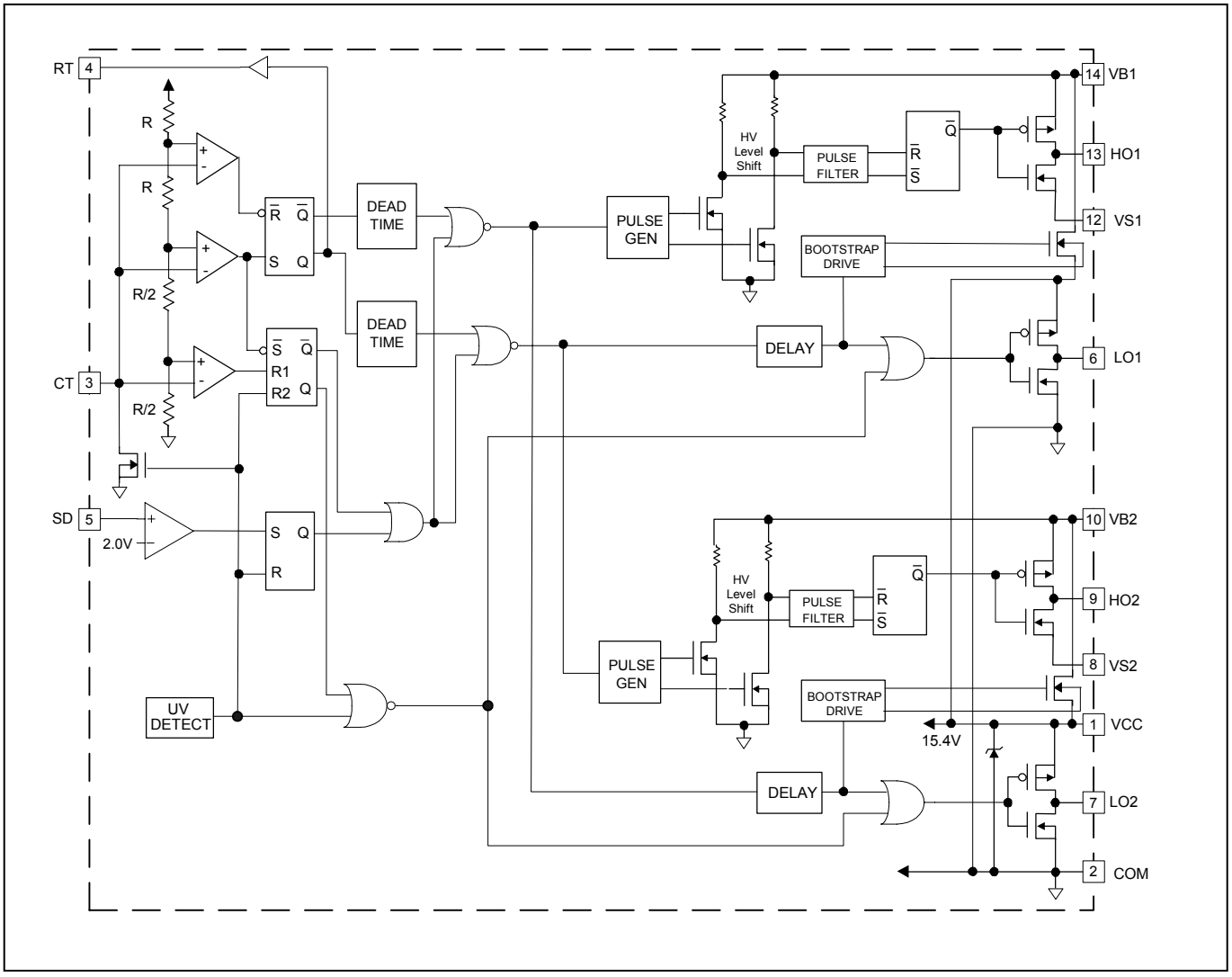
Lead Assignment



Lead Definitions

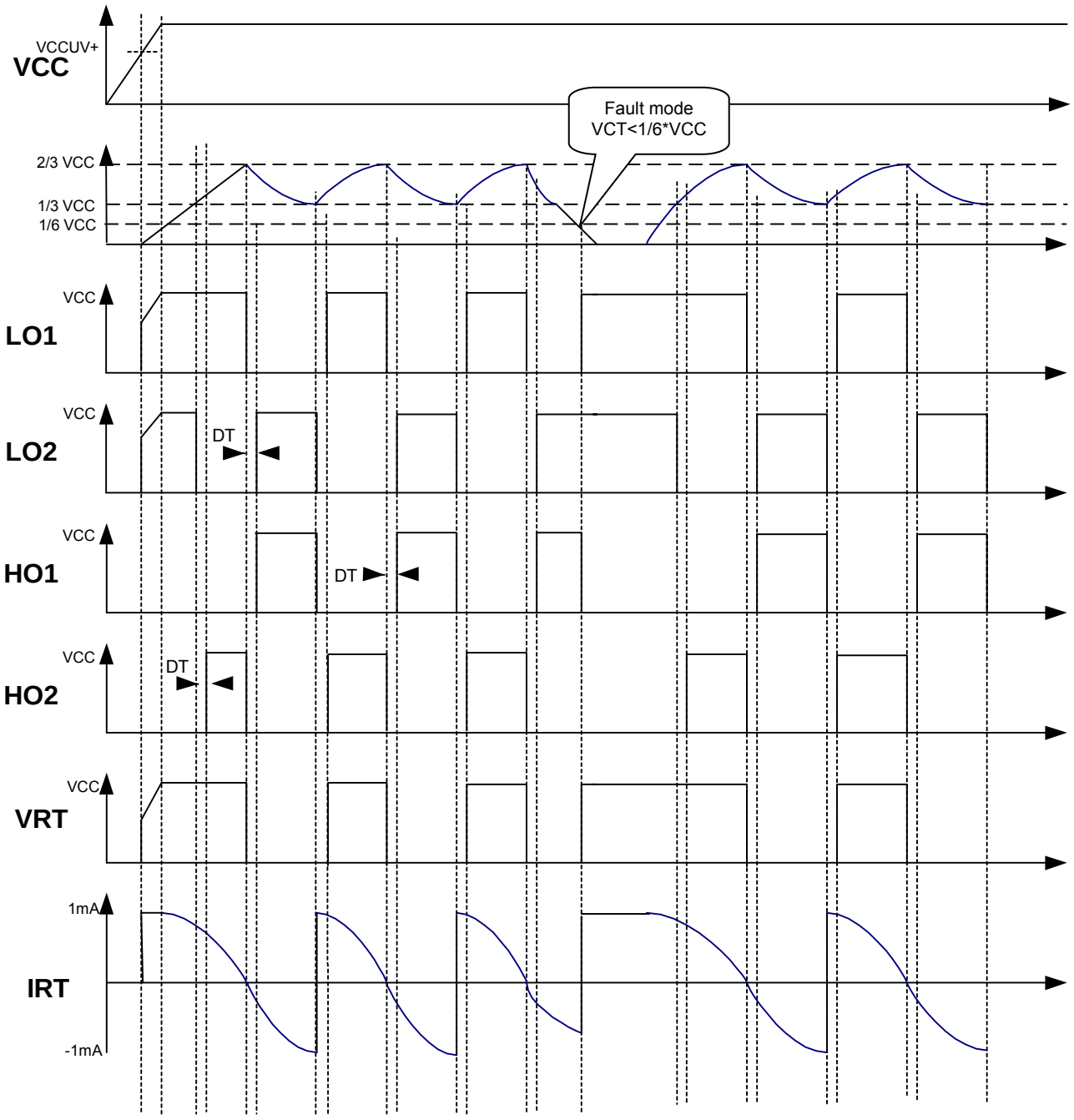
Lead		
Pin	**Symbol**	**Description**
1	VCC	Logic and internal gate drive supply voltage
2	COM	IC power and signal ground
3	CT	Oscillator timing capacitor input
4	RT	Oscillator timing resistor input
5	SD	Shutdown input
6	LO1	Low side gate driver output
7	LO2	Low side gate driver output
8	VS2	High voltage floating supply return
9	HO2	High side gate driver output
10	VB1	High side gate driver floating supply
11	NC	No connect
12	VS1	High voltage floating supply return
13	HO1	High side gate driver output
14	VB1	High side gate driver floating supply

Functional Block Diagram



All values are typical.

Timing Diagram



Functional Description

Under-Voltage Lock-Out Mode (UVLO)

The under-voltage lockout mode (UVLO) is defined as the state the IC is in when V_{CC} is below the turn-on threshold of the IC. The IRS2453D under-voltage lock-out is designed to maintain an ultra low supply current of less than 150 μA, and to guarantee the IC is fully functional before the high and low side output drivers are activated. During under-voltage lock-out mode, the high and low side driver outputs LO1, LO2, HO1, HO2 are all low. With V_{CC} above the V_{CCUV+} threshold, the IC turns on and the output begin to oscillate.

Normal Operating Mode

Once V_{CC} reaches the start-up threshold V_{CCUV+}, the MOSFET M1 opens, RT increases to approximately V_{CC} (V_{CC}-V_{RT+}) and the external CT capacitor starts charging. Once the CT voltage reaches V_{CT-} (about 1/3 of V_{CC}), established by an internal resistor ladder, LO1 and HO2 turn on with a delay equivalent to the deadtime (t_d). Once the CT voltage reaches V_{CT+} (approximately 2/3 of V_{CC}), LO1 and HO2 go low, RT goes down to approximately ground (V_{RT-}), the CT capacitor starts discharging and the deadtime circuit is activated. At the end of the deadtime, LO2 and HO1 go high. Once the CT voltage reaches V_{CT-}, LO2 and HO1 go low, RT goes to high again, the deadtime is activated. At the end of the deadtime, LO1 and HO2 go high and the cycle starts over again.

The frequency is best determined by the graph, Frequency vs. RT, page 3, for different values of CT. A first order approximate of the oscillator frequency can also be calculated by the following formula::

$$f \approx \frac{1}{1.453 \times RT \times CT}$$

This equation can vary slightly from actual measurements due to internal comparator over- and under-shoot delays.

Bootstrap MOSFET

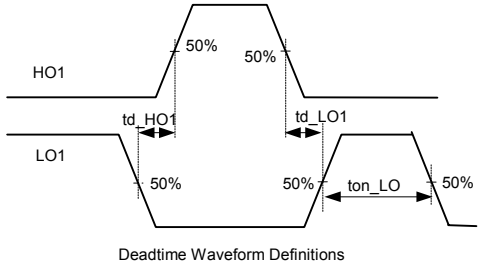
The internal bootstrap FET and supply capacitor (C_{BOOT}) comprise the supply voltage for the high side driver circuitry. The internal boostrap FET only turns on when the corresponding LO is high. To guarantee that the high-side supply is charged up before the first pulse on HO1 and HO2, LO1 and LO2 are both on when CT ramps between zero and 1/3*V_{CC}. LO1 and LO2 are also on when CT is grounded below 1/6*V_{CC} to ensure that the bootstrap capacitor is charged when CT is brought back over 1/3*V_{CC}.

Non-Latched Shutdown

If CT is pulled down below V_{CTSD} (approximately 1/6 of V_{CC}) by an external circuit, CT doesn't charge up and oscillation stops. All outputs are held low and the bootstrap FETs are off. Oscillation will resume once CT is able to charge up again to V_{CT-}.

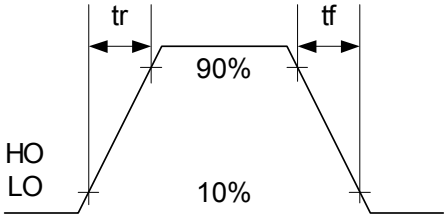
Latched Shutdown

When the SD pin is brought above 2 V, the IC goes into fault mode and all outputs are low. V_{CC} has to be recycled below V_{CCUV-} to restart the IC. The SD pin can be used for over-current or over-voltage protection using appropriate external circuitry.

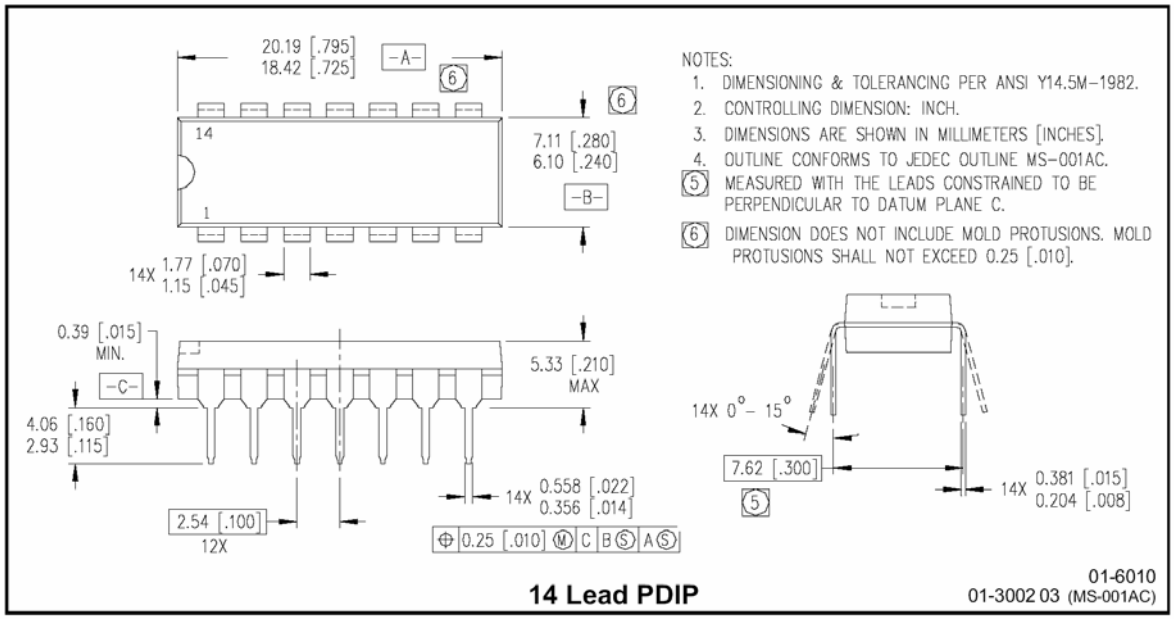


Deadtime Waveform Definitions

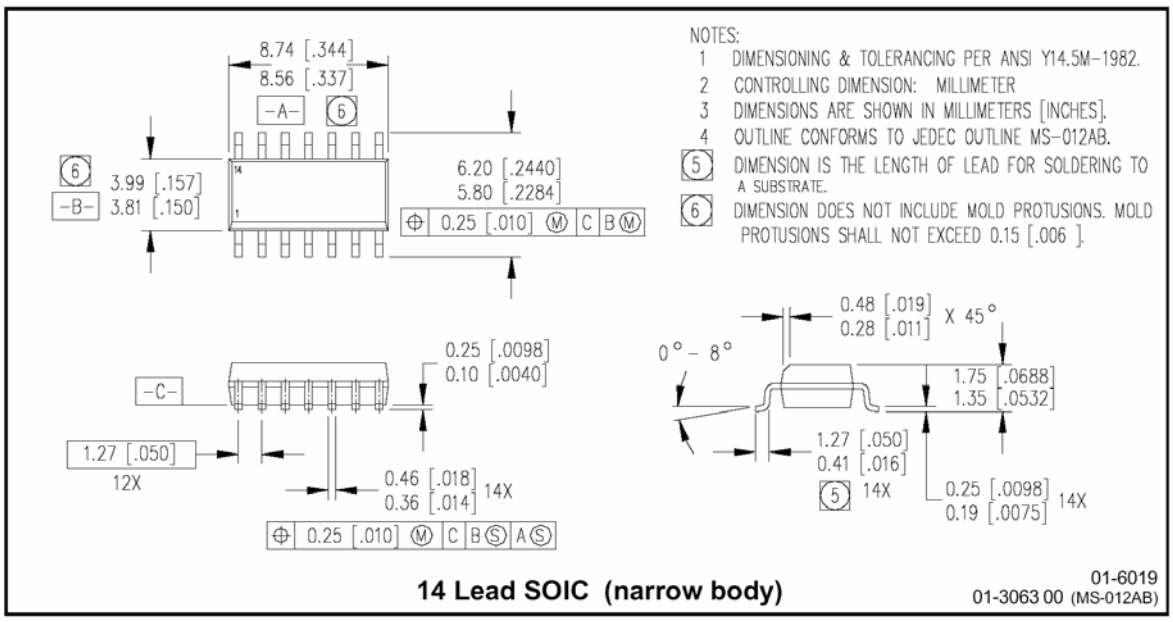
Deadtime Waveform



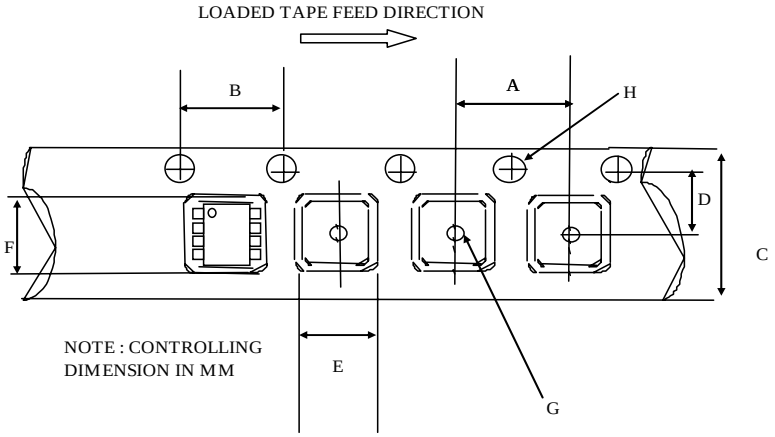
Rise and Fall Time Waveform



IRS2453D

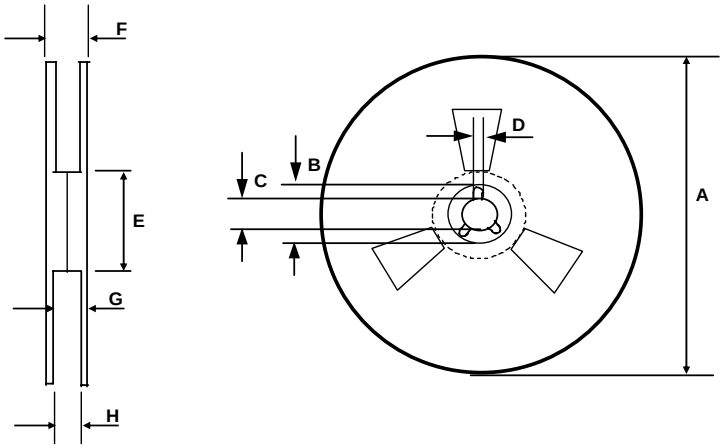


IRS2453DS



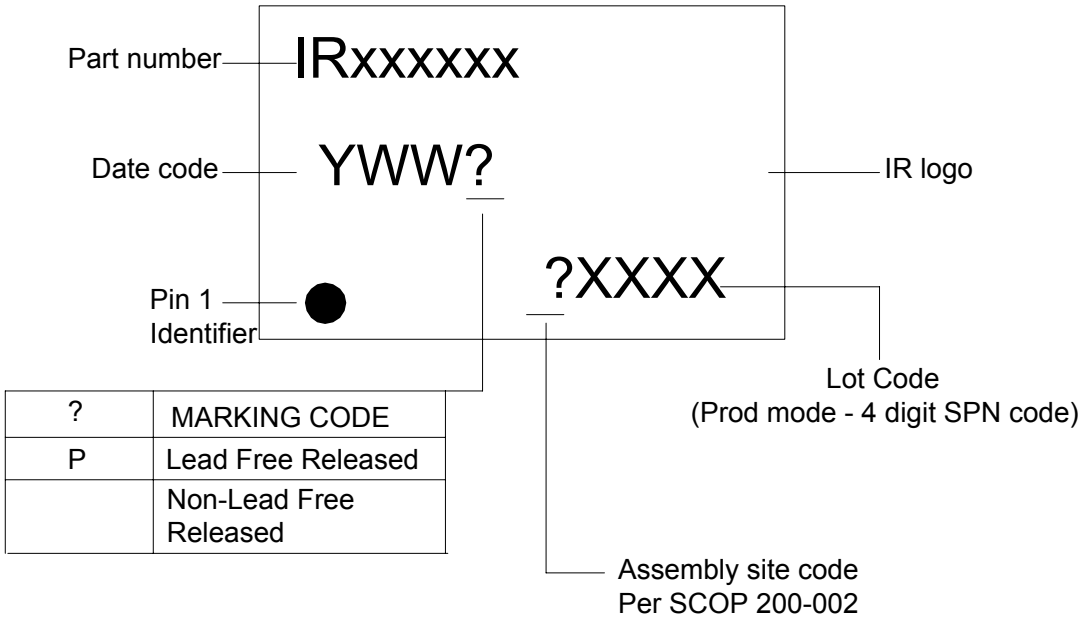
CARRIER TAPE DIMENSION FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

14-lead PDIP IRS2453DPbF
14-lead SOIC IRS2453DSPbF
14-lead SOIC tape & reel IRS2453DSTRPbF

The SOIC-14 is MSL3 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com <http://www.irf.com/>
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

REVISION HISTORY

February 20, 2006

		July '05 revision			Feb '06 revision			
Symbol	Definition	Min	Typ	Max	Min	Typ	Max	Units
Supply Characteristics								
V_{CCUV+}	Rising V_{CC} undervoltage lockout threshold	10.0	11.0	12.0	10.0	11.0	12.0	V
V_{CCUV-}	Falling V_{CC} undervoltage lockout threshold	7.8	8.8	9.8	8.0	9.0	10.0	
$V_{CCUVHYS}$	V_{CC} undervoltage lockout hysteresis	0.5	1.0	1.5	1.6	2.0	2.4	
V_{CLAMP}	V_{CC} Zener clamp voltage	14.9	15.9	16.9	14.6	15.6	16.6	
Oscillator I/O Characteristics								
f_{OSC}	Oscillator frequency (R_T=36.5 kΩ)	18.6	19.2	19.8	19.6	20.2	20.8	kHz
	Oscillator frequency (R_T=7.15 kΩ)	85	91	97	89	95	101	
V_{CT+}	Upper C_T ramp voltage threshold	---	9.33	---	---	9.1	---	V
V_{CT-}	Lower C_T ramp voltage threshold	---	4.66	---	---	4.8	---	
t_r	Output rise time	---	100	150	---	120	220	ns
I_{O+}	Output source current	---	200	---	---	180	---	mA
I_{O-}	Output sink current	---	400	---	---	260	---	
Bootstrap FET Characteristics								
V_{B1_ON} V_{B2_ON}	V_B when the bootstrap FET is on	---	14	---	---	13.7	---	V
I_{B1_CAP} I_{B2_CAP}	V_B source current when FET is on	---	50	---	30	55	---	mA
$I_{B1\_10\ V}$ $I_{B2\_10\ V}$	V_B source current when FET is on	---	10	---	8	12	---	

June 30, 2006

		June '06 revision			Feb '06 revision			
Symbol	Definition	Min	Typ	Max	Min	Typ	Max	Units
Supply Characteristics								
$V_{CCUVHYS}$	V_{CC} undervoltage lockout hysteresis	1.5	2.0	2.4	1.6	2.0	2.4	V
I_{CC_20K}	V_{CC} supply current at f_{OSC} (R_T = 36.5 kΩ)	---	3.0	3.5	Not specified			mA
I_{CCFLT}	V_{CC} supply current when SD>V_{SD}	---	360	500	Not specified			µA
I_{QBS1}, I_{QBS2}	Quiescent V_{BS} supply current	---	30	100	---	60	100	
Oscillator I/O Characteristics								
f_{OSC}	Oscillator frequency (R_T=7.15 kΩ)	88	94	100	89	95	101	kHz
V_{CT+}	Upper C_T ramp voltage threshold	---	9.3	---	---	9.1	---	V
V_{CT-}	Lower C_T ramp voltage threshold	---	4.7	---	---	4.8	---	
t_r	Output rise time	---	120	200	---	120	220	ns
Gate Driver Output Characteristics								
t_d	Output deadtime (HO or LO)	0.8	1.0	1.40	0.75	1.0	1.50	µs
t_{sd}	Shutdown propagation delay	---	250	---	---	275	---	
Shutdown Characteristics								
V_{SD}	Shutdown threshold at SD pin (latched)	1.8	2.0	2.3	---	2.0	---	V
V_{CTSD}	C_T voltage shutdown threshold (non latched)	2.2	2.3	2.5	---	2.3	---	
Bootstrap FET Characteristics								
V_{B1_ON} V_{B2_ON}	V_B when the bootstrap FET is on	13.7	14.0	---	---	13.7	---	V
I_{B1_CAP} I_{B2_CAP}	V_B source current when FET is on	40	55	---	30	55	---	mA
$I_{B1\_10\ V}$ $I_{B2\_10\ V}$	V_B source current when FET is on	10	12	---	8	12	---	